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1 Multi-level texture caching for 3D graphics hardware

Michael Cox, Narendra Bhandari, Michael Shantz

April 1998 **ACM SIGARCH Computer Architecture News , Proceedings of the 25th annual international symposium on Computer architecture**, Volume 26 Issue 3

Full text available: pdf(1.62 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Traditional graphics hardware architectures implement what we call the *push architecture* for texture mapping. Local memory is dedicated to the accelerator for fast local retrieval of texture during rasterization, and the application is responsible for managing this memory. The push architecture has a bandwidth advantage, but disadvantages of limited texture capacity, escalation of accelerator memory requirements (and therefore cost), and poor memory utilization. The push architecture also ...

2 TriangleCaster: extensions to 3D-texturing units for accelerated volume rendering

Gunter Knittel

July 1999 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available: pdf(1.49 MB) Additional Information: full citation, references, citings, index terms

Keywords: 3D-texture mapping, graphics hardware, ray casting, volume rendering

3 The design and analysis of a cache architecture for texture mapping

Ziyad S. Hakura, Anoop Gupta

May 1997 **ACM SIGARCH Computer Architecture News , Proceedings of the 24th annual international symposium on Computer architecture**, Volume 25 Issue 2

Full text available: pdf(2.10 MB) Additional Information: full citation, abstract, references, citings, index terms

The effectiveness of texture mapping in enhancing the realism of computer generated imagery has made support for real-time texture mapping a critical part of graphics pipelines. Despite a recent surge in interest in three-dimensional graphics from computer architects, high-quality high-speed texture mapping has so far been confined to costly hardware systems that use brute-force techniques to achieve high performance. One obstacle faced by designers of texture mapping systems is the requirement ...

4 Evaluation of high performance multicache parallel texture mapping
Alexis Vartanian, Jean-Luc Béchennec, Nathalie Drach-Temam
July 1998 **Proceedings of the 12th international conference on Supercomputing**
Full text available: pdf(1.06 MB) Additional Information: full citation, references, citings, index terms

5 Neon: a single-chip 3D workstation graphics accelerator
Joel McCormack, Robert McNamara, Christopher Gianos, Larry Seiler, Norman P. Jouppi, Ken Correll
August 1998 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**
Full text available: pdf(1.58 MB) Additional Information: full citation, references, citings, index terms

Keywords: chunk rendering, direct rendering, graphics pipeline, level of detail, rasterization, texture cache, tile rendering

6 Parallel texture caching
Homan Igehy, Matthew Eldridge, Pat Hanrahan
July 1999 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**
Full text available: pdf(1.80 MB) Additional Information: full citation, references, citings, index terms

7 Multi-resolution representations: Interactive visualization of unstructured grids using hierarchical 3D textures
Joshua Leven, Jason Corso, Jonathan Cohen, Subodh Kumar
October 2002 **Proceedings of the 2002 IEEE symposium on Volume visualization and graphics**
Full text available: pdf(2.83 MB) Additional Information: full citation, abstract, references, index terms

We present a system for interactively rendering large, unstructured grids. Our approach is to voxelize the grid into a 3D voxel octree, and then to render the data using hierarchical, 3D texture mapping. This approach leverages the current 3D texture mapping PC hardware for the problem of unstructured grid rendering. We specialize the 3D texture octree to the task of rendering unstructured grids through a novel *pad and stencil* algorithm, which distinguishes between data and non-data voxel ...

8 Texture mapping: Resample hardware for 3D graphics
Koen Meinds, Bart Barenbrug
September 2002 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS conference on Graphics hardware**
Full text available: pdf(909.72 KB) Additional Information: full citation, abstract, references, index terms

Texture mapping is a core technology of current real-time 3D graphics systems. To avoid aliasing artifacts, the texture mapping resample process requires proper filtering. We present a new resample algorithm for two-pass forward texture mapping that is suited to an efficient hardware implementation. This method delivers high quality anti-aliased images using filter techniques based on digital signal processing. We use an input sample driven texture resample and filtering algorithm that "splats" ...

9 Prefetching in a texture cache architecture
Homan Igehy, Matthew Eldridge, Kekoa Proudfoot
August 1998 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**
Full text available: pdf(1.45 MB) Additional Information: full citation, references, citings, index terms

10 Radiance interpolants for accelerated bounded-error ray tracing
Kavita Bala, Julie Dorsey, Seth Teller
July 1999 **ACM Transactions on Graphics (TOG)**, Volume 18 Issue 3
Full text available: pdf(888.58 KB) Additional Information: full citation, abstract, references, citings, index terms, review

Ray tracers, which sample radiance, are usually regarded as offline rendering algorithms that are too slow for interactive use. In this article we present a system that exploits object-space, ray-space, image-space, and temporal coherence to accelerate ray tracing. Our system uses per-surface interpolants to approximate radiance both interactive and batch ray tracers. Our approach explicity decouples the two primary operations of a ray tracer—shading and visibility de ...

Keywords: 4D interpolation, approximation, data structures, error bounds, interactive, interval arithmetic, radiance, rendering, rendering systems, visibility

11 Multimedia and graphics: ZR: a 3D API transparent technology for chunk rendering
Emile Hsieh, Vladimir Pentkovski, Thomas Piazza
December 2001 **Proceedings of the 34th annual ACM/IEEE international symposium on Microarchitecture**
Full text available: pdf(765.52 KB) Publisher Site Additional Information: full citation, abstract, references

This paper presents ZR (Zone Rendering), a 3D graphics technology that addresses ever-increasing bandwidth requirements using chunk rendering technique, and at the same time solves 3D API compatibility issues commonly associated with chunk rendering graphics devices. We apply a pipeline serialization technique to handle the cases causing compatibility issues. However, excessive frequency of serializations may offset the performance advantage of ZR. In order to manage potential performance proble ...

12 Application-adaptive intelligent cache memory system
Jung-Hoon Lee, Shin-Dug Kim, Charles Weems
November 2002 **ACM Transactions on Embedded Computing Systems (TECS)**, Volume 1 Issue 1
Full text available: pdf(1.10 MB) Additional Information: full citation, abstract, references, citings, index terms

This article presents the design of a simple hardware-controlled, high performance cache system. The design supports fast access time, optimal utilization of temporal and spatial localities adaptive to given applications, and a simple dynamic fetching mechanism with different fetch sizes. Support for dynamically varying the fetch size makes the cache equally effective for general-purpose as well as multimedia applications. Our cache organization and operational mechanism are especially designed ...

Keywords: Memory hierarchy, dynamic block fetching and cache memory, general application, media application, spatial locality, temporal locality

13 Gigabyte volume viewing using split software/hardware interpolation
William R. Volz
October 2000 **Proceedings of the 2000 IEEE symposium on Volume visualization**
Full text available: pdf(917.24 KB) Additional Information: full citation, references, citings, index terms

Keywords: large datasets, texturing, trilinear interpolation

14 Dynamic 3D graphics workload characterization and the architectural implications
Tulika Mitra, Tzi-cker Chiueh
November 1999 **Proceedings of the 32nd annual ACM/IEEE international symposium on Microarchitecture**
Full text available: pdf(1.05 MB) Publisher Site Additional Information: full citation, abstract, references, citings, index terms

Although PC-class 3D graphics hardware has made significant strides in the last several years, the underlying architectural design principles are still generally considered as a black art. The quantitative approach prevalent in mainstream computer architecture design is rarely applied, at least as far as publicly available research literature is concerned. One main reason for this deficiency is the absence of a detailed workload characterization of 3D applications. This paper report ...

15 Hardware: Hexagonal storage scheme for interleaved frame buffers and textures
Yosuke Bando, Takahiro Saito, Masahiro Fujita
July 2005 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS conference on Graphics hardware HWWS '05**
Full text available: pdf(703.31 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a storage scheme which statically assigns pixel/texel coordinates to multiple memory banks in order to minimize frame buffer and texture memory access load imbalance. In this scheme, the pixels stored in a particular memory bank are placed at the center and the vertices of hexagons packed in the frame buffer By making these hexagons close to regular so that the pixel placement is uniform and isotropic, frame buffer and texture memory accesses are evenly distributed over the m ...

16 Accelerating time-varying hardware volume rendering using TSP trees and color-based error metrics
David Ellsworth, Ling-Jen Chiang, Han-Wei Shen
October 2000 **Proceedings of the 2000 IEEE symposium on Volume visualization**
Full text available: pdf(305.84 KB) Additional Information: full citation, references, citings, index terms

Keywords: graphics hardware, scalar field visualization, time-varying fields, volume rendering, volume visualization

17 Cache performance for multimedia applications
Nathan T. Slingerland, Alan Jay Smith
June 2001 **Proceedings of the 15th international conference on Supercomputing**
Full text available: pdf(642.63 KB) Additional Information: full citation, abstract, references, citings, index terms

The caching behavior of multimedia applications has been described as having high

instruction reference locality within small loops, very large working sets, and poor data cache performance due to non-locality of data references. Despite this, there is no published research deriving or measuring these qualities. Utilizing the previously developed Berkeley Multimedia Workload, we present the results of execution driven cache simulations with the goal of aiding future media processing architect ...

Keywords: CPU caches, cache, mulitmedia, simulation, trace driven simulation

18 Talisman: commodity realtime 3D graphics for the PC
Jay Torborg, James T. Kajiya
August 1996 **Proceedings of the 23rd annual conference on Computer graphics and interactive techniques**
Full text available: pdf(107.48 KB) Additional Information: full citation, references, citings, index terms

19 3D RGB image compression for interactive applications
Chandrajit Bajaj, Insung Ihm, Sanghun Park
January 2001 **ACM Transactions on Graphics (TOG)**, Volume 20 Issue 1
Full text available: pdf(2.41 MB) Additional Information: full citation, abstract, references, citings, index terms

This paper presents a new 3D RGB image compression scheme designed for interactive real-time applications. In designing our compression method, we have compromised between two important goals: high compression ratio and fast random access ability, and have tried to minimize the overhead caused during run-time reconstruction. Our compression technique is suitable for applications wherein data are accessed in a somewhat unpredictable fashion, and real-time performance of decompression is nece ...

20 Hierarchical image caching for accelerated walkthroughs of complex environments
Jonathan Shade, Dani Lischinski, David H. Salesin, Tony DeRose, John Snyder
August 1996 **Proceedings of the 23rd annual conference on Computer graphics and interactive techniques**
Full text available: pdf(115.24 KB) Additional Information: full citation, references, citings, index terms

Keywords: BSP-tree, image-based rendering, level-of-detail, path coherence, spatial hierarchy, texture mapping

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